


## EXHIBIT 007

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**


“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
1. Integrated circuit comprising a plurality of processing modules (M, S) said modules being disposed on the same chip, and	<p>Without conceding that the preamble of claim 1 of the '818 Patent is limiting, Qualcomm Incorporated and Qualcomm Technologies, Inc.'s (together, “Qualcomm”) Snapdragon 8+ Gen 1 Mobile Platform (hereinafter, the “Snapdragon SoC”) is an integrated circuit.</p>  <h2 data-bbox="663 451 1606 505">Snapdragon 8+ Gen 1 Mobile Platform</h2> <p data-bbox="512 727 1728 792"><b>New power and performance enhancements deliver the ultimate boost across all your on-device experiences.</b></p> <p data-bbox="512 857 1707 1040">The Snapdragon® 8+ Gen 1 Mobile Platform is our premium-tier powerhouse. Qualcomm® Adreno™ GPU offers a 10% increase in GPU clock speeds and 30% GPU power reduction while the Qualcomm® Kryo™ CPU provides 10% better CPU performance and 30% CPU improved power efficiency. Plus, this platform delivers additional power savings and extended performance across the board—including over 80 minutes longer video streaming and more than 50 minutes longer web browsing.</p> <p data-bbox="512 1101 1871 1170"><a href="https://www.qualcomm.com/products/application/smartphones/snapdragon-8-series-mobile-platforms/snapdragon-8-plus-gen-1-mobile-platform">https://www.qualcomm.com/products/application/smartphones/snapdragon-8-series-mobile-platforms/snapdragon-8-plus-gen-1-mobile-platform</a></p>

<sup>1</sup> The Snapdragon SoC is charted as a representative product made used, sold, offered for sale, and/or imported by or on behalf of Qualcomm. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p>The Snapdragon SoC comprises a plurality of processing modules, for example Qualcomm Adreno GPU; Qualcomm Kryo CPU; Qualcomm Hexagon Processor; and Platform Security Foundations, Trusted Execution Environment &amp; Services, Secure Processing Unit (SPU):</p> <div data-bbox="506 483 898 617">  <p><b>Snapdragon</b> 8+ mobile platform Gen 1</p> </div> <div data-bbox="1457 509 1732 532">SPECIFICATIONS &amp; FEATURES</div> <div data-bbox="506 680 714 704"><b>Artificial Intelligence</b></div> <div data-bbox="506 714 892 966"> <p>Qualcomm® Adreno™ GPU</p> <p>Qualcomm® Kryo™ CPU</p> <p>Qualcomm® Hexagon™ Processor</p> <ul style="list-style-type: none"> <li>Fused AI Accelerator <ul style="list-style-type: none"> <li>Hexagon Tensor Accelerator</li> <li>Hexagon Vector eXtensions</li> <li>Hexagon Scalar Accelerator</li> </ul> </li> <li>Support for mix precision (INT8+INT16)</li> <li>Support for all precisions (INT8, INT16, FP16)</li> </ul> <p>Qualcomm® Sensing Hub</p> </div> <div data-bbox="506 990 735 1015"><b>5G Modem-RF System</b></div> <div data-bbox="506 1024 892 1360"> <p>Snapdragon® X65 5G Modem-RF System</p> <ul style="list-style-type: none"> <li>5G mmWave and sub-6 GHz, standalone</li> <li>(SA) and non-standalone (NSA) modes, FDD, TDD</li> <li>Dynamic Spectrum Sharing</li> <li>mmWave: 8 carriers, 2x2 MIMO</li> <li>Sub-6 GHz: 4x4 MIMO</li> <li>Qualcomm® 5G PowerSave 2.0</li> <li>Qualcomm® Smart Transmit™ 2.0 technology</li> <li>Qualcomm® Wideband Envelope Tracking</li> <li>Qualcomm® AI-Enhanced Signal Boost</li> <li>Global 5G multi-SIM</li> </ul> <p>Downlink: Up to 10 Gbps</p> <p>Multimode support: 5G NR, LTE including CBRS, WCDMA, HSPA, CDMA 1x, EV-DO, GSM/EDGE</p> </div> <div data-bbox="930 680 1014 704"><b>Camera</b></div> <div data-bbox="930 714 1312 1393"> <p>Qualcomm Spectra™ Image Signal Processor</p> <ul style="list-style-type: none"> <li>Triple 18-bit ISPs</li> <li>Up to 3.2 Gigapixels per Second computer vision ISP (CV-ISP)</li> <li>Up to 36 MP triple camera @ 30 FPS with Zero Shutter Lag</li> <li>Up to 64+36 MP dual camera @ 30 FPS with Zero Shutter Lag</li> <li>Up to 108 MP single camera @ 30 FPS with Zero Shutter Lag</li> <li>Up to 200 Megapixel Photo Capture</li> </ul> <p>Rec. 2020 color gamut photo and video capture</p> <p>Up to 10-bit color depth photo and video capture</p> <p>8K HDR Video Capture + 64 MP Photo Capture</p> <p>10-bit HEIF: HEIC photo capture, HEVC video capture</p> <p>Video Capture Formats: HDR10+, HDR10, HLG, Dolby Vision</p> <p>8K HDR Video Capture @ 30 FPS</p> <p>4K Video Capture @ 120 FPS</p> <p>Slow-mo video capture at 720p @ 960 FPS</p> <p>Bokeh Engine for Video Capture</p> <p>Video super resolution</p> <p>Multi-frame Noise Reduction (MFNR)</p> <p>Locally Motion Compensated Temporal Filtering</p> <p>Multi-Frame and triple exposure staggered/digital overlap HDR dual-sensor support</p> <p>AI-based face detection, auto-focus, and auto-exposure</p> </div> <div data-bbox="1344 680 1400 704"><b>CPU</b></div> <div data-bbox="1344 714 1732 784"> <p>Kryo CPU</p> <ul style="list-style-type: none"> <li>Up to 3.2 GHz*, with Arm Cortex-X2 technology</li> <li>64-bit Architecture</li> </ul> </div> <div data-bbox="1344 812 1526 837"><b>Visual Subsystem</b></div> <div data-bbox="1344 846 1732 1115"> <p>Adreno GPU</p> <ul style="list-style-type: none"> <li>Vulkan® 1.1 API support</li> <li>HDR gaming (10-bit color depth, Rec. 2020 color gamut)</li> <li>Physically Based Rendering</li> <li>Volumetric Rendering</li> <li>Adreno Frame Motion Engine</li> <li>API Support: OpenGL® ES 3.2, OpenCL™ 2.0 FP, Vulkan 1.1</li> <li>Hardware-accelerated H.265 and VP9 decoder</li> <li>HDR Playback Codec support for HDR10+, HDR10, HLG and Dolby Vision</li> </ul> </div> <div data-bbox="1344 1144 1434 1170"><b>Security</b></div> <div data-bbox="1344 1179 1732 1365"> <p>Platform Security Foundations, Trusted Execution Environment &amp; Services, Secure Processing Unit (SPU)</p> <p>Trust Management Engine</p> <p>Qualcomm® wireless edge services (WES) and premium security features</p> <p>Qualcomm® 3D Sonic Sensor and Qualcomm® 3D Sonic Max (fingerprint sensor)</p> <p>Qualcomm® Type-1 Hypervisor</p> </div>

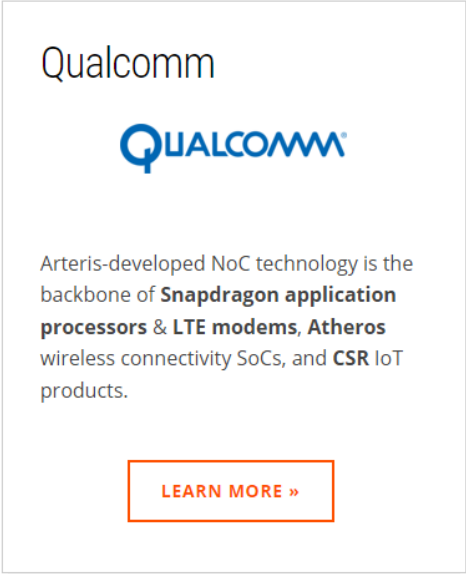
**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p><b>Wi-Fi &amp; Bluetooth™</b></p> <p>Qualcomm® FastConnect™ 6900 System</p> <ul style="list-style-type: none"> <li>• Wi-Fi Standards: Wi-Fi 6E, Wi-Fi 6 (802.11ax),</li> <li>• Wi-Fi 5 (802.11ac), 802.11a/b/g/n</li> <li>• Wi-Fi Spectral Bands: 24 GHz, 5 GHz, 6 GHz</li> <li>• Peak speed: 3.6 Gbps</li> <li>• Channel Bandwidth: 20/40/80/160 MHz</li> <li>• 8-stream sounding (for 8x8 MU-MIMO)</li> <li>• MIMO Configuration: 2x2 (2-stream)</li> <li>• MU-MIMO (Uplink &amp; Downlink)</li> <li>• 4K QAM</li> <li>• OFDMA (Uplink &amp; Downlink)</li> <li>• 4-Stream (2x2 + 2x2) Dual Band Simultaneous (DBS)</li> <li>• Wi-Fi Security: WPA3-Enterprise, WPA3- Enhanced Open, WPA3 Easy Connect, WPA3-Personal</li> </ul> <p><b>Integrated Bluetooth</b></p> <ul style="list-style-type: none"> <li>• Bluetooth Features: Bluetooth® 5.3, LE Audio, Dual Bluetooth antennas</li> <li>• Bluetooth audio: Snapdragon Sound™ Technology with support for Qualcomm® aptX™ Voice, aptX Lossless, aptX Adaptive, and LE audio</li> </ul> <p><b>snapdragon.com</b></p> <p><small>*Snapdragon 8+ Gen 1 Mobile Platform also available in 3 GHz CPU version. Maximum CPU speed will vary based on platform version. Consult OEM specifications for device CPU speed. Certain optional features available subject to Carrier and OEM selection for an additional fee. Snapdragon, Qualcomm, Qualcomm Hexagon, Qualcomm SG PowerSave, Qualcomm Kiya, Qualcomm Smart Transmit, Qualcomm Wideband Envelope Tracking, Qualcomm AI Enhanced Signal Boost, Qualcomm Spectra, Qualcomm Adreno, Qualcomm 3D Sonic Sensor, Qualcomm Type1 Hypervisor, Qualcomm Adreno, Qualcomm Sensing Hub, Qualcomm 3D Sonic Max, Qualcomm FastConnect, Snapdragon Sound, Qualcomm aptX, Snapdragon Elite Gaming, and Qualcomm Quick Charge are products of Qualcomm Technologies, Inc. and/or its subsidiaries. Qualcomm wireless edge services are offered by Qualcomm Technologies Inc. and/or its subsidiaries. Snapdragon, Qualcomm, Hexagon, Snapdragon Elite Gaming, Adreno, FastConnect, Snapdragon Sound, Kiya, Smart Transmit, Qualcomm Spectra, Qualcomm Adreno, Snapdragon Sight, and Quick Charge are trademarks or registered trademarks of Qualcomm Incorporated. aptX is a trademark or registered trademark of Qualcomm Technologies International, Ltd. ©2022 Qualcomm Technologies, Inc. and/or its affiliated companies. All Rights Reserved.</small></p> <p><a href="https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/Snapdragon-8-plus-Gen-1-Product-Brief.pdf">https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/Snapdragon-8-plus-Gen-1-Product-Brief.pdf</a></p>
a network (N; RN) arranged for providing at least one connection between a first and	<p><b>Audio</b></p> <p>Qualcomm Aqstic™ audio codec (WCD9385)</p> <p>New Qualcomm Aqstic smart speaker amplifier (WSA8835)</p> <p>Total Harmonic Distortion + Noise (THD+N), Playback: -108dB</p> <p>Qualcomm® Audio and Voice Communication Suite</p> <p><b>Display</b></p> <p>On-Device Display Support:</p> <ul style="list-style-type: none"> <li>• 4K @ 60 Hz</li> <li>• QHD+ @ 144 Hz</li> </ul> <p>Maximum External Display Support:</p> <ul style="list-style-type: none"> <li>• up to 4K @ 60 Hz</li> <li>• 10-bit color depth, Rec. 2020 color gamut</li> <li>• HDR10 and HDR10+</li> </ul> <p>Demura and subpixel rendering for OLED Uniformity</p> <p><b>Charging</b></p> <p>Qualcomm® Quick Charge™ 5 Technology</p> <p><b>Location</b></p> <p>GPS, Glonass, BeiDou, Galileo, QZSS, NavIC capable</p> <p>Dual Frequency GNSS (L1/L5)</p> <p>Sensor-Assisted Positioning</p> <ul style="list-style-type: none"> <li>• Urban pedestrian navigation with sidewalk accuracy</li> <li>• Global freeway lane-level vehicle navigation</li> </ul> <p><b>Memory</b></p> <p>Support for LP-DDR5 memory up to 3200 MHz</p> <p>Memory Density: up to 16 GB</p> <p><b>General Specifications</b></p> <p>Full Suite of Snapdragon Elite Gaming™ features</p> <p>4 nm Process Technology</p> <p>USB Version 3.1; USB Type-C Support</p> <p>Part Number: SM8475</p> <p>Without conceding that the preamble of claim 1 of the '818 Patent is limiting, the Snapdragon SoC utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the “Arteris NoC”) as a network (N; RN) arranged for providing connections between a first and at least one second module (M, S) in the Snapdragon SoC, wherein said modules communicate via a network on chip, either literally or under the doctrine of equivalents.</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
<p>at least one second module (M, S), wherein said modules communicate via a network on chip, and</p>	<p>The Snapdragon SoC utilizes utilizing the Arteris NoC as a data communication network:</p> <div data-bbox="510 414 972 984">  <p>Qualcomm</p> <p>Arteris-developed NoC technology is the backbone of <b>Snapdragon application processors &amp; LTE modems, Atheros wireless connectivity SoCs, and CSR IoT products.</b></p> <p><a href="#">LEARN MORE »</a></p> </div> <p><a href="https://web.archive.org/web/20210514110614/https://www.arteris.com/customers">https://web.archive.org/web/20210514110614/https://www.arteris.com/customers</a></p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p data-bbox="583 293 1495 345">Certain Arteris Technology Assets Acquired</p> <p data-bbox="827 381 1251 410">by <b>Kurt Shuler</b>, on October 31, 2013</p> <p data-bbox="512 457 1373 487">Arteris to continue to license, support and maintain Arteris FlexNoC® interconnect IP</p> <p data-bbox="512 516 1562 636">SUNNYVALE, California — October 31, 2013 — Arteris Inc., a leading innovator and supplier of silicon-proven commercial <b>network-on-chip (NoC) interconnect IP</b> solutions, today announced that Qualcomm Technologies, Inc. (“Qualcomm”), a subsidiary of Qualcomm Incorporated, has acquired certain technology assets from Arteris and hired personnel formerly employed by Arteris.</p> <p data-bbox="512 678 1495 847"> <b>“</b>Arteris NoC technology has been and will continue to be a key enabler for creating larger and more complex chips in a shorter amount of time at a lower cost. This acquisition of our technology assets represents a validation of the value of Arteris’ Network-on-Chip interconnect IP technology.         <b>”</b> </p> <p data-bbox="1352 896 1516 925"><b>ARTERIS<sup>IP</sup></b></p> <p data-bbox="1213 984 1516 1003"><i>K. Charles Janac, President and CEO, Arteris</i></p> <p data-bbox="512 1062 1528 1247">As part of the acquisition transaction, Arteris retains the right to license, support and maintain the existing <b>Arteris FlexNoC</b> and Arteris FlexLLI product lines in order to fulfill existing and new licensing contracts. Qualcomm has agreed to make certain FlexNoC updates available to Arteris based upon an agreed upon schedule and provide certain engineering support to Arteris. Arteris has rights to make customer support-related modifications to FlexNoC. There are no changes in Arteris’ contractual obligations or operations with customers or industry partners.</p> <p data-bbox="512 1299 1797 1370"> <a href="https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31">https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31</a>;  <a href="https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team">https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team</a> </p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p>In the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p> <p><b>11.3.1.1 Transaction Layer</b></p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> <li>• A master sends request packets.</li> <li>• Then, the slave returns response packets.</li> </ul> <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

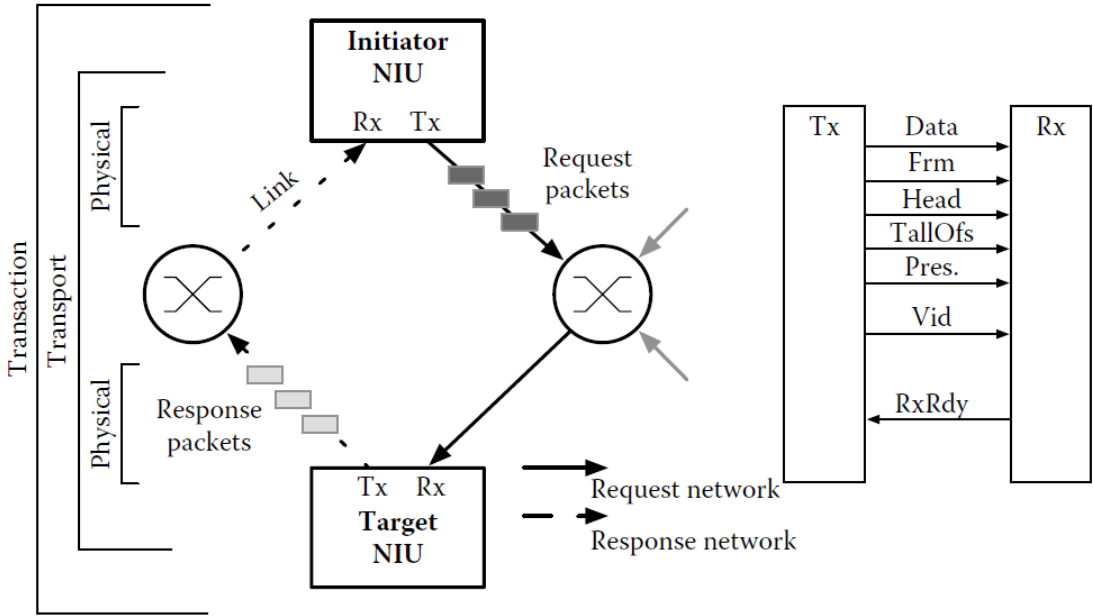
“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>



**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	 <p><b>FIGURE 11.1</b> NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 312-313; see <i>id</i> at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: “In this chapter we will present an MPSoC platform [...] using Arteris NoC as communication infrastructure.”).</p> <p>A large SoC, such as the Snapdragon SoC may include multiple classes of Arteris NoC:</p>

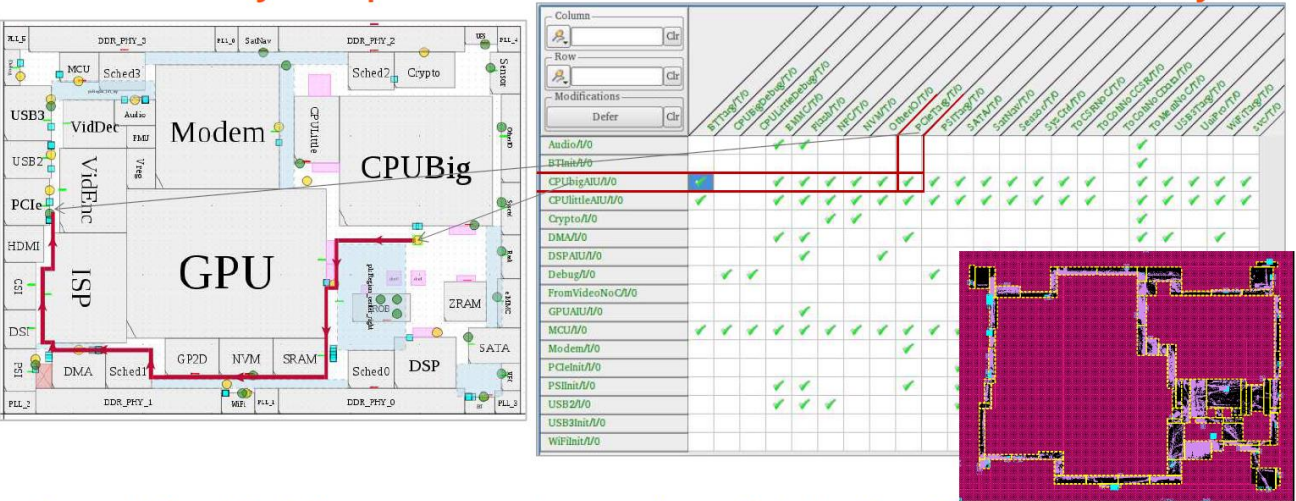
**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<div data-bbox="525 300 1575 357"> <h2>Logical Interconnect Topology Development</h2> </div> <div data-bbox="525 365 1407 397"> <h3>FLEXNOC &amp; NCORE INTERCONNECT IPS DEFINE ARCHITECTURES</h3> </div> <div data-bbox="525 406 1092 828"> <p>The diagram illustrates the Main Interconnect architecture, showing various IP blocks (CPU, GPU, DSP, MMU, etc.) connected to a central Main Interconnect. It also shows Cache Coherent Interconnect and Memory NoC components.</p> </div> <div data-bbox="1092 406 1491 763"> <p>Two diagrams showing Ncore Cache Coherent NoC and Memory NoC topologies, illustrating the network-on-chip architecture.</p> </div> <div data-bbox="1491 373 1869 844"> <p>Three diagrams showing Main NoC, Service NoC, and Video NoC topologies, illustrating the network-on-chip architecture.</p> </div> <div data-bbox="525 844 1743 958"> <ul style="list-style-type: none"> <li>• ArChip16 Example: Large SoCs have multiple classes of interconnect             <ul style="list-style-type: none"> <li>– Non-coherent, Coherent, Control/Status, Observability, etc.</li> </ul> </li> <li>• Ncore &amp; FlexNoC interconnects are managed separately from IP blocks, increasing design flexibility</li> </ul> </div> <div data-bbox="499 974 1879 1031"> <div> </div> <div>             ISPD 2018, 28 March 2018         </div> <div>             Copyright © 2018 Arteris IP   9         </div> </div> <div data-bbox="489 1075 1894 1149" data-label="Text"> <p>See Physical Interconnect Aware Network Optimizer, <a href="http://www.ispd.cc/slides/2018/s7_2.pdf">http://www.ispd.cc/slides/2018/s7_2.pdf</a>, at slide 9.</p> </div> <div data-bbox="489 1193 1894 1273" data-label="Text"> <p>As a further illustration, connections between modules within the Arteris NoC may be defined by a connectivity table:</p> </div>

## U.S. Patent No. 7,366,818 (Radulescu &amp; Goossens)

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p data-bbox="541 310 1829 362"><b>Connectivity Map → Interconnect Connections → Layout</b></p>  <ul data-bbox="541 860 1829 974" style="list-style-type: none"> <li>• Connectivity table defines interconnect connections within the floorplan</li> <li>• Routes must pass through available channels in the floorplan</li> <li>• Connectivity passes from initiator NIU to switch, to link, to RC buffers and finally to target NIU</li> </ul> <p data-bbox="1661 868 1829 893">DC-Topographical</p> <p data-bbox="512 1008 642 1032"><b>ARTERIS IP</b></p> <p data-bbox="1115 1015 1262 1029">ISPD 2018, 28 March 2018</p> <p data-bbox="1667 1015 1877 1029">Copyright © 2018 Arteris IP   12</p> <p data-bbox="504 1063 1877 1133">See Physical Interconnect Aware Network Optimizer, <a href="http://www.ispd.cc/slides/2018/s7_2.pdf">http://www.ispd.cc/slides/2018/s7_2.pdf</a>, at slide 12.</p> <p data-bbox="205 1144 474 1380">wherein said connection supports transactions comprising outgoing messages</p> <p data-bbox="504 1144 1877 1380">The Arteris NoC utilized by the Snapdragon SoC has a connection that supports transactions comprising outgoing messages from the first module to the second modules and return messages from the second modules to the first module, either literally or under the doctrine of equivalents.</p> <p data-bbox="504 1295 1877 1372">For example, in the Arteris NoC, “[m]ost transactions require the following two-step transfers,” including “[a] master send[ing] request packets” and “the slave return[ing] response packets”:</p>

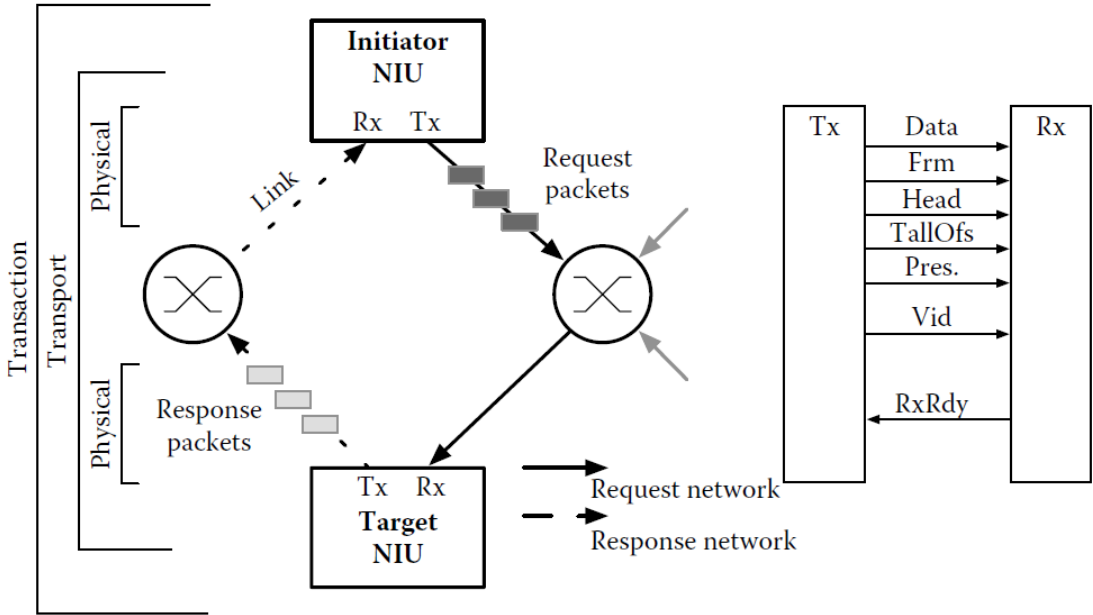
**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

’818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
<p>from the first module to the second modules and return messages from the second modules to the first module</p>	<p><b>11.3.1.1 Transaction Layer</b></p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> <li>• A master sends request packets.</li> <li>• Then, the slave returns response packets.</li> </ul> <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets</p> <p>on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU’s Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	 <p><b>FIGURE 11.1</b> NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 312-313.</p>
the integrated circuit comprising at least one dropping means (DM) for dropping data exchanged by	<p>The Arteris NoC utilized by the Snapdragon SoC has at least one dropping means (DM) for dropping data exchanged by said first and second module (M, S), either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC addresses packet corruption using, among other mechanisms, “packet validity checker” and “initiator timeout,” which may result in data being dropped:</p>



**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim

said first and second module (M, S), and

Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip<sup>1</sup>

Example NoC Functional Safety Mechanisms

Function	Failure Modes	Safety Mechanisms
Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; Initiator timeout
Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout
Clocking and reset	Clock / reset glitch; Frequency error;	External Timeout AoU;
	Wrong clock gating	Initiator timeout; Packet validity checker; Percentage safe AoU
Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU
Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU

Functions

Failure Modes

Safety Mechanisms

10

© 2018 Arm Limited

ARTERIS<sup>IP</sup>

+

arm

Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP, <https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation>, at 10.

As a further example, the Arteris NoC includes “packet validity checking” and “transaction timeout” for error resiliency, which may result in data being dropped:

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p><i>A. Advanced Data Protection and Reliability for SoC Interconnects</i></p> <p>Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller.</p> <p>The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent.</p> <p>Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP, <a href="https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf">https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf</a> at 7.</p> <p>As a further example, in the Arteris NoC, “[t]arget-side timeout in the network interface units detects unresponsive target IP failures and ensures that they do not block the NoC,” which may result in data being dropped:</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p><i>C. Transaction Timeout</i></p> <p>Target-side timeout in network interface units detects unresponsive target IP failures and ensures that they do not block the NoC. Initiator-side timeout in network interface units detects transport packet deletion, bad routing, or failures of stuck arbiters or targets. Timeout is detected per transaction using a pre-scaled counter to minimized hardware cost and power consumption.</p> <p>SoC Reliability Features in the FlexNoC Resilience Package, <a href="http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf">http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf</a> at 2.</p>
<p>at least one interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN),</p>	<p>The Arteris NoC utilized by the Snapdragon SoC has at least one interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN), either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which “translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols” and in the Arteris NoC, the NIUs “are at the boundary of the NoC” and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:</p>



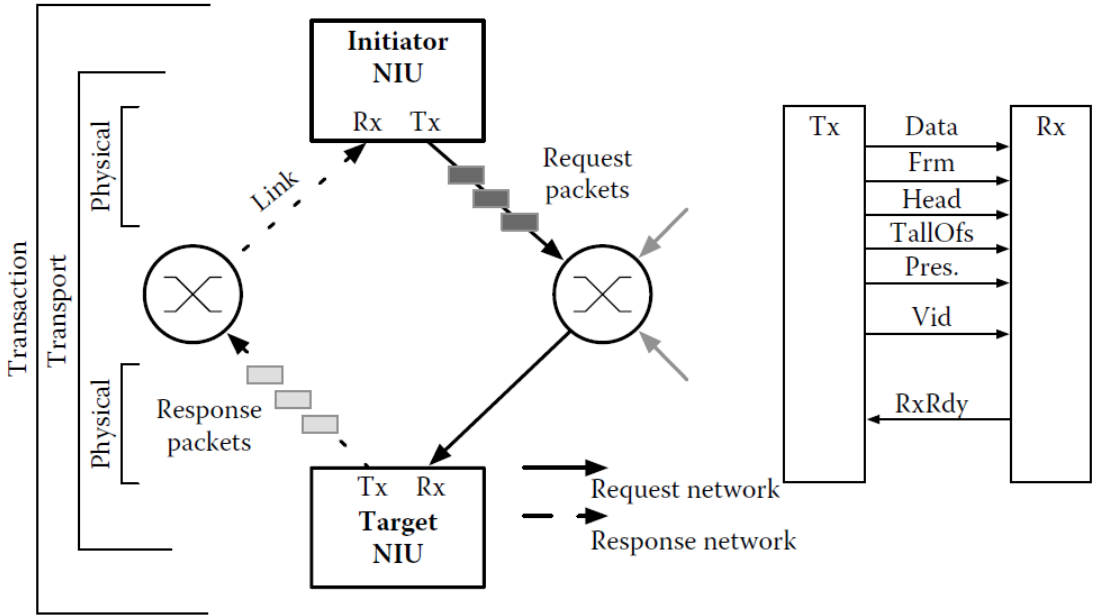
**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

’818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p><b>11.3.1.1 Transaction Layer</b></p> <p>The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers:</p> <ul style="list-style-type: none"> <li>• A master sends request packets.</li> <li>• Then, the slave returns response packets.</li> </ul> <p>As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU’s Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	 <p><b>FIGURE 11.1</b> NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.</p> <p>See Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 311, 312-313.</p> <p>The Initiator NIUs are “used to connect a master node to the NoC,” and the Target NIUs are “used to connect a slave node to the NoC”:</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p><b>11.3.2 Network Interface Units</b></p> <p>The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul style="list-style-type: none"> <li>• <b>Initiator NIU</b>—third party protocol-to-NTTP, used to connect a master node to the NoC</li> <li>• <b>Target NIUs</b>—NTTP-to-third party protocol, used to connect a slave node to the NoC</li> </ul> <p>Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 316-317.</p> <p>In the Arteris NoC “Initiator NIU units...enable connection between an AMBA-AHB master IP and the NoC”:</p>

## U.S. Patent No. 7,366,818 (Radulescu &amp; Goossens)

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p><b>11.3.2.1 Initiator NIU Units</b></p> <p>Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU.</p> <p>A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p>burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is</p> <ul style="list-style-type: none"> <li>• During a read request, until the requested data arrives from the Rx port</li> <li>• During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received</li> <li>• When an internal FIFO is full</li> </ul>

## U.S. Patent No. 7,366,818 (Radulescu &amp; Goossens)

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p style="text-align: center;"><b>NIU Architecture</b></p> <p>The diagram illustrates the NIU Architecture, which is divided into two main sections: the Request Path and the Response Path. Both paths interface with an AHB Slave Interface on the left. The Request Path starts with an AHB Req signal entering the AHB Slave Interface. Data flows from the AHB Slave Interface into a DATA FIFO, then to a Packet Assembly block, and finally to a PIPE bw/lw block, which connects to the Tx Port. The Response Path starts with an AHB Resp signal entering the AHB Slave Interface. Data flows from the Rx Port into a WIDTH CONVERTER (dashed box), then to a PIPE block, and finally to a FLOW CONTROL block. The FLOW CONTROL block sends information back to the AHB Slave Interface. Additionally, there is a CONTROL signal path from the Rx Port area back to the FLOW CONTROL block. A TRANSLATION TABLE and BUILD HEADER &amp; NECKER block are also shown, connected to the AHB Slave Interface and the Request Path.</p> <p><b>FIGURE 11.4</b> Network interface unit: Initiator architecture.</p> <p>Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 317-318.</p> <p>As further example, “Target NIU units enable connection of a slave IP to the NoC by translating</p>



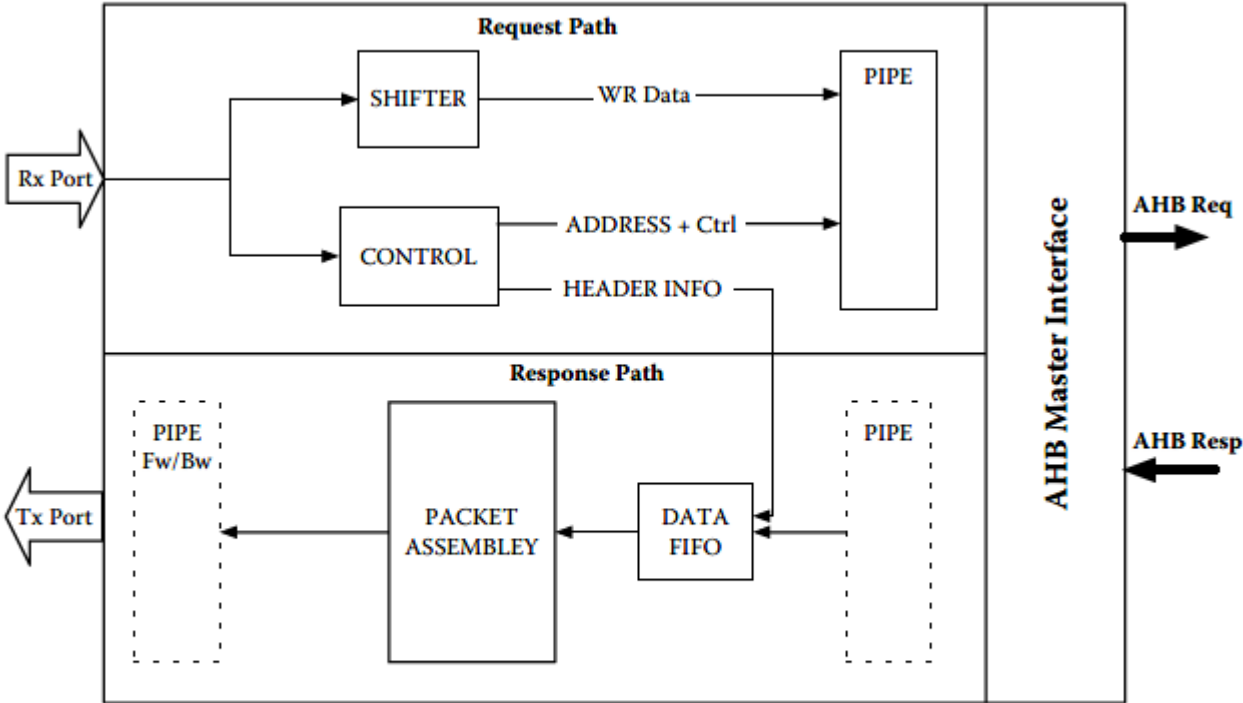
**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p>NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets”:</p> <p><b>11.3.2.2 Target NIU Units</b></p> <p>Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always 32 bits wide, but the actual address space size may be downsized by setting a hardware parameter. Unused AHB address bits are then driven to zero. The NTTP request packet is then translated into one or more corresponding AHB accesses, depending on the transaction type (word aligned or nonaligned access). For example, if the request is an atomic Store, or a Load that can fit an AHB burst of specified length, then such a burst is generated. Otherwise, an AHB burst with unspecified length is generated.</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p style="text-align: center;"><b>Target NIU Architecture</b></p>  <p>The diagram illustrates the Target NIU Architecture. It is divided into two main horizontal sections: the Request Path (top) and the Response Path (bottom). On the left, there is an Rx Port (input) and a Tx Port (output). The Request Path includes a SHIFTER block that receives data from the Rx Port and outputs WR Data to a PIPE block. A CONTROL block also receives data from the Rx Port and outputs ADDRESS + Ctrl and HEADER INFO to the same PIPE block. The Response Path includes a DATA FIFO block that receives data from the PIPE block and outputs to a PACKET ASSEMBLY block. The PACKET ASSEMBLY block then outputs to a dashed box labeled PIPE Fw/Bw, which connects to the Tx Port. A vertical AHB Master Interface block is positioned to the right of the main processing blocks, with AHB Req (request) and AHB Resp (response) signals passing through it.</p> <p><b>FIGURE 11.5</b> Network interface unit: Target architecture.</p> <p>Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 318-319.</p>



**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

’818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
<p>wherein said interface means (ANIP, PNIP) comprises a first dropping means (DM) for dropping data, and</p>	<p>The interface means of the Arteris NoC utilized by the Snapdragon SoC comprises a first dropping means (DM) for dropping data, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which include Initiator NIUs, that are “used to connect a master node to the NoC,” and the Target NIUs, that are “used to connect a slave node to the NoC”:</p> <p><b>11.3.2 Network Interface Units</b></p> <p>The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p> <ul style="list-style-type: none"> <li>• <b>Initiator NIU</b>—third party protocol-to-NTTP, used to connect a master node to the NoC</li> <li>• <b>Target NIUs</b>—NTTP-to-third party protocol, used to connect a slave node to the NoC</li> </ul> <p>Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 316-317.</p> <p>For example, the Arteris NoC addresses packet corruption using, among other mechanisms, “packet validity checker” and “initiator timeout,” which may result in data being dropped:</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim

Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip<sup>1</sup>

Example NoC Functional Safety Mechanisms

Function	Failure Modes	Safety Mechanisms
Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; Initiator timeout
Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout
Clocking and reset	Clock / reset glitch; Frequency error;	External Timeout AoU;
	Wrong clock gating	Initiator timeout; Packet validity checker; Percentage safe AoU
Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU
Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU

Functions

Failure Modes

Safety Mechanisms

10

© 2018 Arm Limited

ARTERISIP

+

arm

Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP,

<https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation>, at 10.

As a further example, the Arteris NoC “can pass IP-generated error-correcting code (ECC) information through the NoC between the socket interfaces” and includes “packet validity checking” and “transaction timeout” for error resiliency, which may result in data being dropped:

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p><i>A. Advanced Data Protection and Reliability for SoC Interconnects</i></p> <p>Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller.</p> <p>The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent.</p> <p>Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP, <a href="https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf">https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf</a> at 7.</p> <p>As a further example, in the Arteris NoC, “[t]arget-side timeout in the network interface units detects unresponsive target IP failures and ensures that they do not block the NoC,” which may result in data being dropped:</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

’818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p><i>C. Transaction Timeout</i></p> <p>Target-side timeout in network interface units detects unresponsive target IP failures and ensures that they do not block the NoC. Initiator-side timeout in network interface units detects transport packet deletion, bad routing, or failures of stuck arbiters or targets. Timeout is detected per transaction using a pre-scaled counter to minimized hardware cost and power consumption.</p> <p>SoC Reliability Features in the FlexNoC Resilience Package, <a href="http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf">http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf</a> at 2.</p>
<p>wherein the dropping of data and therefore the transaction completion can be controlled by the interface means.</p>	<p>In the Arteris NoC utilized by the Snapdragon SoC, the transaction completion can be controlled by the interface means, either literally or under the doctrine of equivalents.</p> <p>For example, the Arteris NoC uses Network Interface Units (NIUs), which include Initiator NIUs, that are “used to connect a master node to the NoC,” and the Target NIUs, that are “used to connect a slave node to the NoC”:</p> <p><b>11.3.2 Network Interface Units</b></p> <p>The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<ul style="list-style-type: none"> <li>• <b>Initiator NIU</b>—third party protocol-to-NTTP, used to connect a master node to the NoC</li> <li>• <b>Target NIUs</b>—NTTP-to-third party protocol, used to connect a slave node to the NoC</li> </ul> <p>Networks-On-Chips Theory and Practice, <a href="https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0">https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0</a>, at 316-317.</p> <p>For example, the Arteris NoC addresses packet corruption using, among other mechanisms, “packet validity checker” and “initiator timeout,” which may result in data being dropped:</p>

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim

Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip<sup>1</sup>

Example NoC Functional Safety Mechanisms

Function	Failure Modes	Safety Mechanisms
Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; Initiator timeout
Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout
Clocking and reset	Clock / reset glitch; Frequency error;	External Timeout AoU;
	Wrong clock gating	Initiator timeout; Packet validity checker; Percentage safe AoU
Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU
Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU

Functions

Failure Modes

Safety Mechanisms

10

© 2018 Arm Limited

ARTERIS<sup>IP</sup>

+

arm

Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP,

<https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation>, at 10.

As a further example, the Arteris NoC “can pass IP-generated error-correcting code (ECC) information through the NoC between the socket interfaces” and includes “packet validity checking” and “transaction timeout” for error resiliency, which may result in data being dropped:

**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p><i>A. Advanced Data Protection and Reliability for SoC Interconnects</i></p> <p>Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller.</p> <p>The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent.</p> <p>Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP, <a href="https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf">https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf</a> at 7.</p> <p>As a further example, in the Arteris NoC, “[t]arget-side timeout in the network interface units detects unresponsive target IP failures and ensures that they do not block the NoC,” which may result in data being dropped:</p>



**U.S. Patent No. 7,366,818 (Radulescu & Goossens)**

“Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same”

'818 Patent Claim	Qualcomm Snapdragon 8+ Gen 1 Mobile Platform System on Chip <sup>1</sup>
	<p><i>C. Transaction Timeout</i></p> <p>Target-side timeout in network interface units detects unresponsive target IP failures and ensures that they do not block the NoC. Initiator-side timeout in network interface units detects transport packet deletion, bad routing, or failures of stuck arbiters or targets. Timeout is detected per transaction using a pre-scaled counter to minimized hardware cost and power consumption.</p> <p>SoC Reliability Features in the FlexNoC Resilience Package, <a href="http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf">http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf</a> at 2.</p>